Claims

1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a test pattern and an actual circuit pattern on a semiconductor substrate by a predetermined semiconductor manufacturing process;

measuring a feature of the three-dimensional shape of said test pattern formed on said semiconductor substrate by use of an optical scatterometry apparatus; and

evaluating said semiconductor manufacturing process for said actual circuit pattern on said semiconductor substrate based on a result of said measurement.

2. A method of manufacturing a semiconductor device as set forth in claim 1, wherein said predetermined semiconductor manufacturing process is an exposure and development process.

3. A method of manufacturing a semiconductor device as set forth in claim 1, wherein said predetermined semiconductor manufacturing process is an etching process.

4. A method of manufacturing a semiconductor device, comprising:

a preparation step comprising the steps of:

preliminarily forming a sample wafer provided with a test pattern and an actual circuit pattern while

varying a process parameter in a semiconductor manufacturing process;

measuring a feature of the three-dimensional shape of said test pattern formed as said sample wafer and a feature of the three-dimensional shape of a predetermined portion of an actual circuit pattern formed as said sample wafer; and

calculating and preparing a correspondence relationship between said three-dimensional shape feature of said test pattern and said three-dimensional shape feature of said predetermined portion of said actual circuit pattern measured while varying said process parameter; and

an evaluation step comprising the steps of:

measuring a feature of the three-dimensional shape of a test pattern formed in a product semiconductor device by use of an optical scatterometry apparatus, at the time of manufacturing said product semiconductor device by forming said test pattern and an actual circuit pattern by a predetermined product semiconductor manufacturing process; and

evaluating said semiconductor manufacturing process for said actual circuit pattern of said product semiconductor device from said correspondence relationship at the time of varying said process parameter prepared in

said preparation step, based on said measured feature of said three-dimensional shape of said test pattern.

5. A method of manufacturing a semiconductor device as set forth in claim 4, wherein in said preparation step, said measurement of said feature of said three-dimensional shape of said test pattern and said feature of said three-dimensional shape of said predetermined portion of said actual circuit pattern is carried out by an AFM observation.

6. A method of manufacturing a semiconductor device as set forth in claim 4, wherein in said preparation step, said measurement of said feature of said three-dimensional shape of said test pattern is carried out by use of an optical scatterometry apparatus, and said measurement of said feature of said three-dimensional shape of said predetermined portion of said actual circuit pattern is carried out by an AFM observation or a cross sectional SEM observation.

7. A method of manufacturing a semiconductor device as set forth in claim 4, wherein in said preparation step and said evaluation step, said semiconductor manufacturing process is a semiconductor exposure and development step, and said process parameter in said semiconductor manufacturing process is at least one selected from the group consisting of an amount of exposure and a focus value.

8. A method of manufacturing a semiconductor device

as set forth in claim 4, wherein in said preparation step and said evaluation step, said semiconductor manufacturing process is a semiconductor etching process, and said process parameter in said semiconductor manufacturing process is at least one selected from the group consisting of a gas flow rate, pressure variation, and etching time.

9. A method of manufacturing a semiconductor device as set forth in claim 4, wherein a fitting function is used for each said process parameter, in calculating said correspondence relationship between said feature of said three-dimensional shape of said test pattern and said feature of said three-dimensional shape of said predetermined portion of said actual circuit pattern at the time of varying said process parameter, in said preparation step.

10. A method of manufacturing a semiconductor device as set forth in claim 4, wherein a process window set for each said process parameter is used, in calculating said correspondence relationship between said feature of said three-dimensional shape of said test pattern and said feature of said three-dimensional shape of said predetermined portion of said actual circuit pattern at the time of varying said process parameter, in said preparation step.

11. A method of manufacturing a semiconductor device,

comprising:

a preparation step which comprises the steps of preliminarily forming a sample wafer provided with a test pattern and an actual circuit pattern while varying a process parameter in a semiconductor manufacturing process, measuring a feature of a three-dimensional shape of said test pattern formed as said sample wafer and a feature of a three-dimensional shape of a predetermined portion of said actual circuit pattern formed as said sample wafer, and calculating and preparing a correspondence relationship between said feature of said three-dimensional shape of said test pattern and said feature of said three-dimensional shape of said predetermined portion of said actual circuit pattern measured while varying said process parameter; and

an evaluation step which comprises, in manufacturing a product semiconductor device by forming a test pattern and an actual circuit pattern by a predetermined product semiconductor manufacturing process, the steps of measuring a feature of the three-dimensional shape of said test pattern formed in said product semiconductor device by use of an optical scatterometry apparatus, estimating a feature of the three-dimensional shape of a predetermined portion of said actual circuit pattern based on said correspondence relationship at the time of varying said process parameter

prepared in said preparation step, and evaluating said semiconductor manufacturing process for said actual circuit pattern of said product semiconductor device based on said estimated three-dimensional shape feature.

12. A method of manufacturing a semiconductor device, comprising:

a preparation step which comprises the steps of preliminarily forming a sample wafer provided with a test pattern and an actual circuit pattern while varying a process parameter in a semiconductor manufacturing process, measuring a feature of the three-dimensional shape of said test pattern formed as said sample wafer and a feature of the three-dimensional shape of a predetermined portion of said actual circuit pattern formed as said sample pattern, setting a range of said process parameter necessary for said three-dimensional shape feature of said predetermined portion of said actual circuit pattern measured while varying said parameter to satisfy a reference three-dimensional shape feature, and calculating and preparing said measured three-dimensional shape feature of said test pattern in said set range of said process parameter; and

an evaluation step which comprises, in manufacturing a product semiconductor device by forming a test pattern and an actual circuit pattern by a predetermined product semiconductor manufacturing process, the steps of measuring

a feature of the three-dimensional shape of said test pattern formed in said product semiconductor device by use of an optical scatterometry apparatus, judging whether or not said measured three-dimensional shape feature of said test pattern is within said range of said process parameter prepared in said preparation step, based on said calculated three-dimensional shape feature of said test pattern within said range of said process parameter, and thereby evaluating said semiconductor manufacturing process for said actual circuit pattern of said product semiconductor device.

13. A method of manufacturing a semiconductor device as set forth in claim 10, wherein in said preparation step and said evaluation step, a range of said process parameter is said process window.

14. A system for manufacturing a semiconductor device, comprising:

a preparation unit for preliminarily measuring, for a plurality of sample wafers provided with a test pattern and an actual circuit pattern while varying a process parameter in a semiconductor manufacturing process, a feature of the three-dimensional shape of said test pattern and a feature of the three-dimensional shape of a predetermined portion of said actual circuit pattern, and calculating and preparing a correspondence relationship

between said three-dimensional shape feature of said test pattern and said three-dimensional shape feature of said predetermined portion of said actual circuit pattern measured while varying said process parameter; and

an evaluation unit, in manufacturing a product semiconductor device by forming a test pattern and an actual circuit pattern by a predetermined product semiconductor manufacturing process, for measuring a feature of the three-dimensional shape of said test pattern formed in said product semiconductor device by use of an optical scatterometry apparatus, and evaluating said semiconductor manufacturing process for said actual circuit pattern of said product semiconductor device from said correspondence relationship at the time of varying said process parameter prepared by said preparation unit, based on said measured three-dimensional shape feature of said test pattern.

15. A system for manufacturing a semiconductor device as set forth in claim 14, further comprising an unit for feeding back the information on said semiconductor manufacturing process evaluated by said evaluation unit to a manufacturing apparatus.